

ABSTRACT OF THE DISCLOSURE**METAL PROGRAMMABLE SELF-TIMED MEMORIES**

5 A self-timed memory array is disclosed, in which segmentability and metal-
programmability are supported while minimizing layout space. Self-timing row decoder circuits
are placed at the top and bottom of the array adjacent to respective I/O blocks. A self-timing signal
is routed from the top (resp. bottom) of the array to a point halfway down (resp. up) the memory
array and then back to a self-timing row decoder at the top (resp. bottom) of the array. The same
10 approach may also be used to account for the bitline wire delay from the bottom (resp. top) of the
array to the sense amplifiers in the I/O block. Further flexibility in wire routing is provided by
eliminating metal routing layers from unneeded memory cells, and a programmable gate array may
be used to allow an arbitrary word size to be chosen for the memory.